

ACCELERATED IP DEVELOPMENT USING AN AGILE RTL DESIGN FLOW



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INTRODUCTION

In 1970, Dr. Winston Royce presented a paper entitled “Managing the Development of Large Software Systems,” that criticized sequential development because the testing phase, which occurs at the end of the development cycle, is the first event for which timing, storage, input/output transfers, etc., are experienced. Companies that develop IP cores for FPGAs and ASICs are frequently asked to deliver custom “one-off” variations of their standard IP offerings. This is a unique design challenge, when compared to end product development, that puts added pressure on development teams to implement modifications quickly and with high quality. Agile development focuses on keeping code simple, testing often, and delivering functional bits of the application as soon as they’re ready. The results of this “inspect-and-adapt” approach to development greatly reduce both development costs and time to market.

One of the lessons from software adoption of agile is the need to automate the testing. This ensures there are sufficient regression tests that validate subsequent code changes do not break previous working delivered features. High reliability RTL is best achieved through an agile development environment that incorporates design automation for static design verification. While FPGA vendor supplied synthesis and place and route tools do identify many design rule violations, more sophisticated checks are needed earlier in the design processes. Two separate analysis environments are required; RTL Analysis for bus contention, register conflicts, race conditions and CDC (clock domain crossing) analysis to reduce metastability issues by identifying asynchronous clock domains and their crossings.

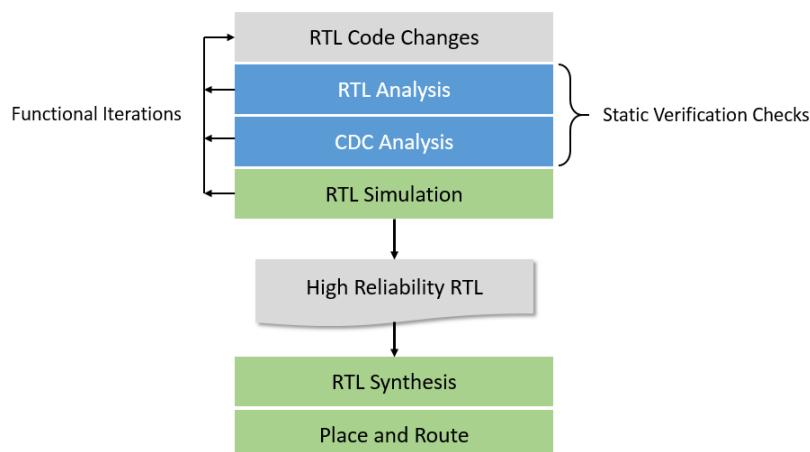


Figure 1 – Agile Design Flow for High Reliability RTL

Without automation, finding and remedying design errors that affect interoperability turns into a random manual exercise. Automation enables an agile design process where developers continuously identify and address design errors while writing the RTL making it easier to develop, easier to test, and more reusable for future designs.

PROMOTE HIGH QUALITY IP TO YOUR CUSTOMERS

Virtually all ASIC and FPGA IP vendors promote the skill and experience of their engineering teams and the high quality of their IP offerings they produce. These somewhat generic claims often fail to establish credible differentiation between vendors with competing products. Additionally, engineers that assemble systems using 3rd party IP are often faced with a significant verification task that is exacerbated by any undetected design rule violations. IP that is developed using an agile development processes that includes static verification checks can claim to be free of design errors, fully tested, contains no unreachable conditional branches or FSM states and is properly registered between all asynchronous clock domains to build confidence and credibility with end customers.

ENABLE END USER SYSTEM VERIFICATION

Analyzing RTL for a single block of a system in isolation is not sufficient to detect all CDC violations but rather the entire system must be considered and analyzed to perform a thorough CDC analysis. However, this can be a challenge for end customers when using 3rd party encrypted IP. Blue Pearl addresses this challenge using a patented technology called “Grey Cell” that enables a representation of a protected IP block for CDC analysis of module-to-module connections while preserving the trade secrets of the original IP provider.

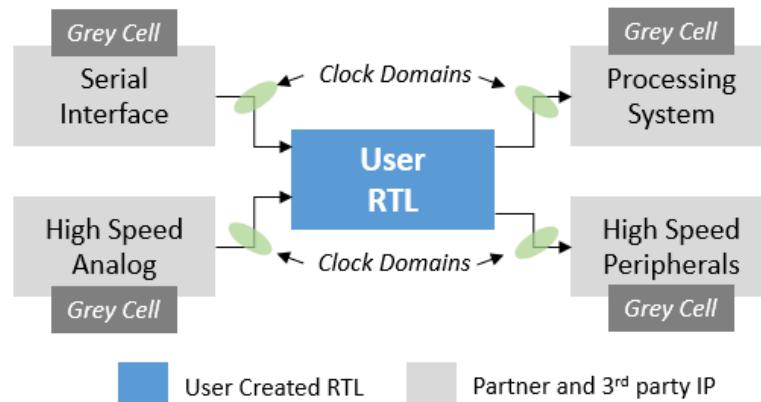


Figure 2 – System Modeling using Grey Cell

By adopting the Blue Pearl static verification suite for FPGA IP development vendors can deliver Grey Cell models of their IP to avoid providing unencrypted RTL to end customers to support this important, system wide CDC analysis.

INDUSTRY'S ONLY STATIC VERIFICATION TOOL OPTIMIZED FOR FPGAS

Blue Pearl offers the only static verification environment optimized for the unique requirements of FPGA design. These checks include analyze for routing congestion, reset configurations and even estimate critical timing paths prior to synthesis. Grey Cell modeling supports the analysis of FPGA vendor provided protected IP cores with asynchronous clock domains. The Visual Verification Suite supports both Xilinx Vivado™ Design Suite with built in UltraFast™ Design Methodology design rules and Altera's Quartus® Prime Design Software and is the only static verification environment that runs on Windows – the preferred FPGA environment.

BLUE PEARL SOFTWARE

Blue Pearl Software, Inc. is a provider of design automation software for ASIC, FPGA and IP RTL verification. Its Analyze RTL™ linting and debug, Clock Domain Crossing analysis and Synopsys Design Constraints (SDC) generation solutions are proven to improve quality-of-results (QoR), reduce risk and decrease development time. The Visual Verification Environment complements RTL simulation solutions provided by EDA and FPGA vendors by ensuring code and SDC quality along with clocking integrity. Engineered to maximize RTL find/fix rates, the Visual Verification Suite uniquely provides easy setup, consistent results, Management Dashboard for complete push-button analytics, and runs on both Linux and Windows.

Blue Pearl Analyze RTL incorporates a suite of technologies into a single RTL analysis environment to help developers find bugs earlier in the design processes. Super-lint tools are combined with the power of formal verification to provide a single, high capacity design checking environment that identifies poor coding styles, improper clocks, simulation and synthesis problems, poor testability and other source code issues. FSM analysis automatically extracts and analyzes finite state machines for dead or terminal states and provides a visual representation. X-propagation analysis will detect unknown states, often introduced into designs to implement soft resets or to implement power management schemes that are masked during RTL simulation. Blue Pearl's CDC Analysis incorporates over a decade of experience to find errors other tools fail to identify.