

# Analyze RTL™

## Overview

The Blue Pearl Software Visual Verification Suite provides enhanced Lint, Debug, Clock Domain Crossing (CDC) and automated SDC generation flows to accelerate ASIC, FPGA and IP RTL Verification on your choice of Linux or Windows.

Analyze RTL™ provides RTL linting combined with a powerful debug environment with the industry's fastest bug find/fix rate to quickly identify critical design issues, up front, streamlining simulation and synthesis while improving overall quality of results.

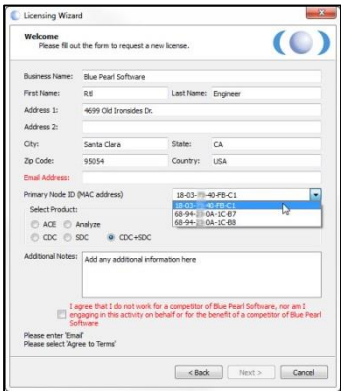
## Key Benefits

Modern ASICs, SoCs and FPGAs routinely have millions of gates with memories, transceivers, third party IP and processor cores. RTL issues can be time consuming and complex to debug in the lab and through simulations. To reduce verification and debug times, Analyze RTL can identify problems quickly before simulation and synthesis, and reducing time in the lab.

## Key Features

Analyze RTL, accelerates RTL verification and debug:

- Fast and meaningful results with tool Setup Wizard



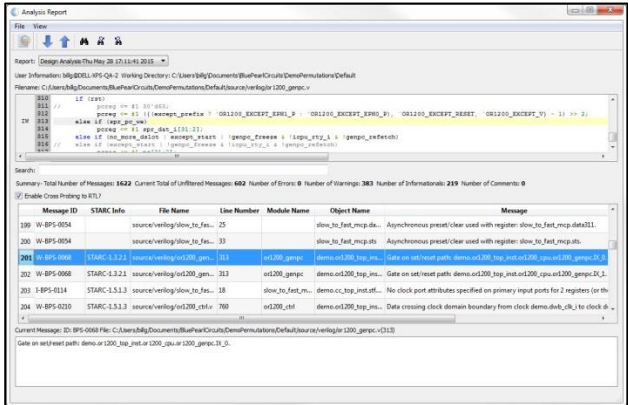
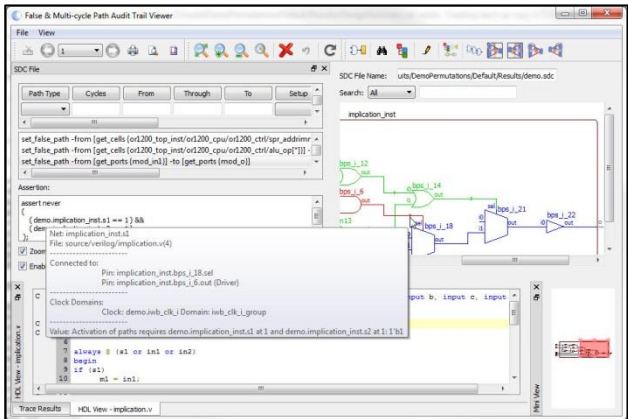
- Check IEEE Verilog/System Verilog & VHDL language specification compliance and syntax

- Configure checks along with standard checks, STARC, RMM, and Xilinx® UltraFast™ Design Methodology
- Integrated RTL, schematics fan-in/out views, object search and message viewer
- Use easy debug message sorting, filtering and waiving to pinpoint problems
- Automated flow with Tcl-based Command Line Interface (CLI), and re-usable message waiver file

## Identify Design Issues Quickly

The Analyze RTL easy setup enables users to debug design issues quickly using intelligent sorting and message filtering.

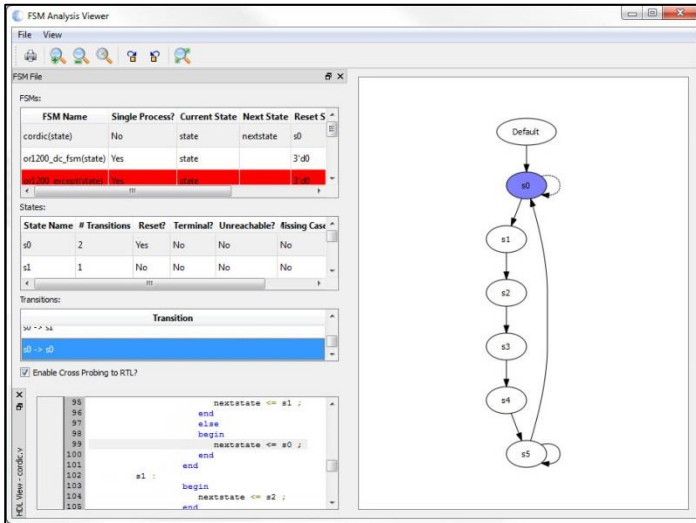
- Low Noise
- Check customization for specific design style
- Waiver migration



## Finite State Machine Analysis

Rather than writing exhaustive simulation test benches to validate their finite state machines (FSMs), designers can use the FSM analysis capability within Analyze RTL. With minimal effort, designers can

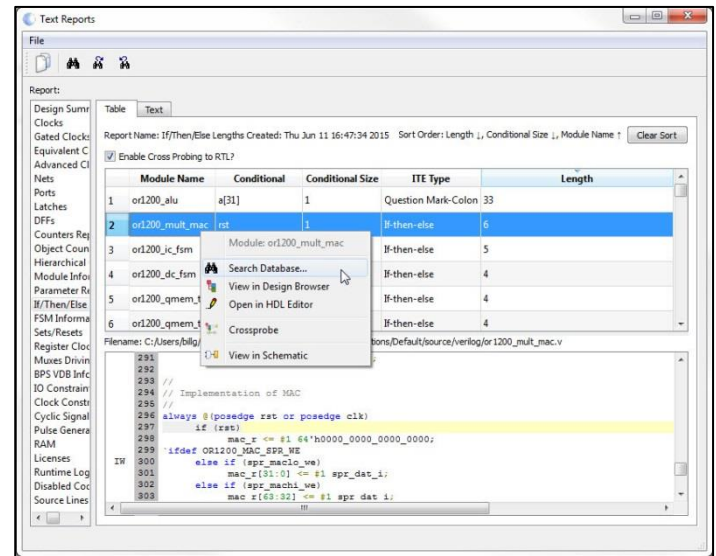
- Extract FSMs from their RTL
- Find dead or unreachable states
- Generate easy to read bubble diagrams to better visualize FSMs



## RTL Checks for High Speed Designs

It is important to find as early as possible RTL coding that prevents the design from getting desired speed. FPGAs, because of their more constrained fabric than ASIC, certain type of structures causes slow down. Rather than wait for synthesis or static timing analysis results, Analyze RTL users can easily identify:

- High fanout nets
- Deep nested “if-then-else” statements
- High levels of logic paths
- Reset methodology, Async/sync



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