



Analyze RTL™

Overview

The Blue Pearl Software Suite is a set of analysis tools for IP and FPGA verification that finds:

- RTL design errors and problems
- Missing Clock Domain Crossing (CDC) synchronization
- Timing false and multi-cycle paths
- Integrates FPGA Vendor checks

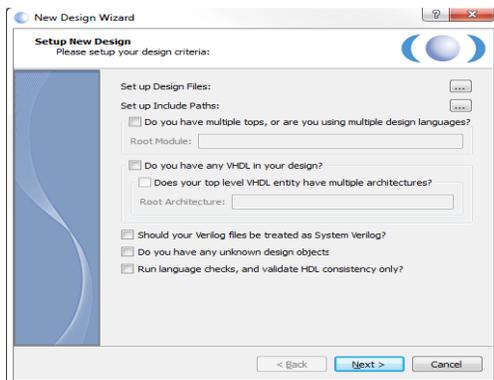
Why Analyze RTL™

FPGAs routinely have millions of gates with memories, transceivers, third party IP and processor cores. Problems can be time consuming and complex to debug in the lab and through simulations. Designers need verification tools that can run before simulation, before synthesis, and definitely before burning chips in the lab, that can identify problems quickly to reduce their verification and debug time.

Features of Analyze RTL™

With Analyze RTL™, designers can

- Get effective and meaningful results quickly with tool Setup Wizard



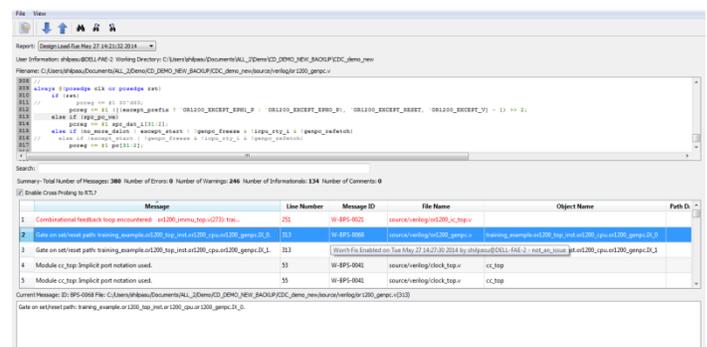
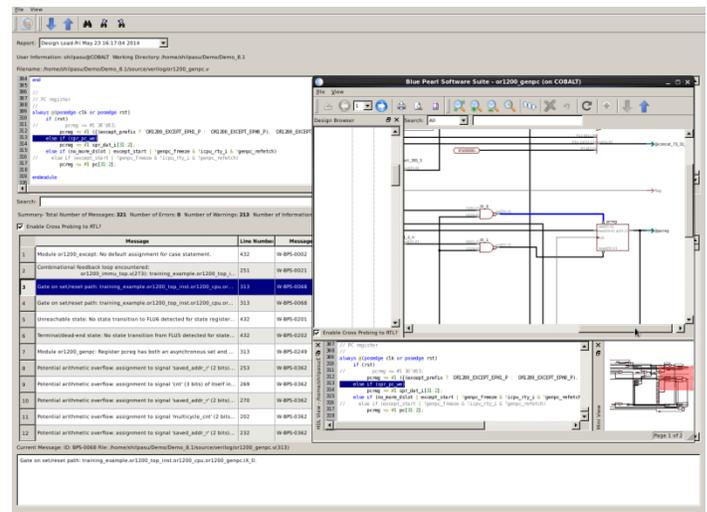
- Check IEEE Verilog/System Verilog & VHDL language specification compliance and syntax
- Configure checks along with standard checks, STARC, RMM, and Xilinx UltraFast

- Use GUI to streamline debug; integrated RTL, Schematic, and message viewer
- Use easy debug message sorting, filtering and waiving to pinpoint problems
- Automate flow with Command Line Interface (CLI), and re-usable message waiver file

Identify Design Issues Quickly

The Visual Verification Environment enables Analyze RTL™ users to debug design issues quickly using intelligent sorting and message filtering.

- Low Noise
- Check customization for specific design style
- Easy setup
- Waiver migration



Finite State Machine Analysis

Rather than writing exhaustive simulation test benches to validate their finite state machines (FSM), designers can use the FSM analysis capability within Analyze RTL™. With minimal effort, designers can

- Extract FSMs from their RTL
- Find dead or unreachable states
- Generate easy to read bubble diagram to better visualize FSM

FSM Analysis Viewer

FSMs:

FSM Name	Single Process?	Current State	Next State	Reset S
or1200_ic_fsm(state)	Yes	state		2'd0
or1200_qmem_top...	Yes	state		3'd0

States:

State Name	# Transitions	Reset?	Terminal?	Unreachable?	Missing Ca
3'd0	3	Yes	No	No	No
3'd1	4	No	No	No	No

Transitions:

Transition
3'd2 -> 3'd1
3'd2 -> 3'd2
3'd2 -> 3'd3

```
351         qmem_dack <= #1 1'b0;
352         qmem_tack <= #1 1'b0;
353     end
354 end
355 OR1200_QMEMFSM_LOAD: begin
356     if (qmemdemu_cycstb_i & daddr_qmem_hit & qmemdcpu_we_i & qmem_ack) begin
357         state <= #1 OR1200_QMEMFSM_STORE;
358         qmem_dack <= #1 1'b1;
359         qmem_tack <= #1 1'b0;
360     end
```

RTL Checks for High Speed Designs

It is important to find as early as possible RTL coding that prevents the design from getting desired speed. FPGAs, because of their more constrained fabric than ASIC, certain type of structures causes slow down. Rather than wait for synthesis or static timing analysis results, Analyze RTL™ users can easily identify

- High fanout nets
- Deep nested “if-then-else” statements
- High levels of logic paths
- Reset methodology, Async/sync

Text Reports

Report Name: Sets/Resets Created: Fri Apr 11 10:40:06 2014 Sort Order: Fanout ↓, Reset/Set Name ↑ Clear Sort

Enable Cross Probing to RTL?

Reset/Set Name	Active	Internal	Fanout
1 demo.rst_i	high	No	2223
2 demo.rst_n	low	No	147
3 demo.iwb_rst_i	high	No	106
4 demo.reset	low	No	105
5 demo.dwb_rst_i	high	No	73
6 demo.rst_la	low	No	4

Filename: C:/Users/billg/Documents/BluePearlCircuits/DemoPermutations/Default/source/verilog/demo.v

```
192 // i/o's for slow_to_fast_mcp
193
194
195 input in_rst;
196 output out;
197
198 //complex_cases synthetic for FPA and MCP
199 //input clk;
200 input rst_n, in1, in2, in3, in4, in5, p_start, A, B, cyclic_input, select, st
201 input [7:0] in1_8;
202 input [7:0] in2_8;
203 output [15:0] out1_16;
204 output [15:0] out2_16;
205 output out1, out2a, out3, out4, out5, out6, out7 ;
206
```

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