IP and FPGA Verification

Blue Pearl Software

CDC Option

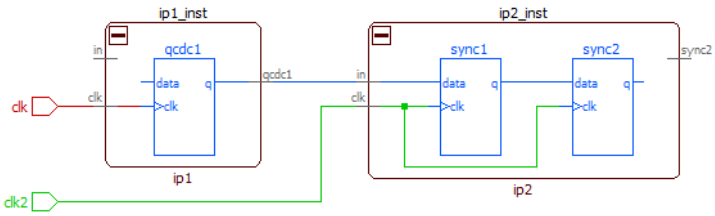
Overview

The Blue Pearl Software Suite offers the capability to analyze designs for Clock Domain Crossing issues:

- Finds places in design that don't have CDC synchronization that cause metastability
- Identifies CDC synchronization types
- Has IP block modeling capability that reduces complexity and accommodates lack of model availability
- Has reports and schematic to understand and debug CDC synchronization
- Easy setup by identifying clocks and FPGA clock generators.
- CDC is an option to Analyze RTL™, the base product within the software suite.

Why CDC Analysis

FPGAs routinely have millions of gates with memories, transceivers, third party IP and processor cores. They have a growing number of clocks that are asynchronous to each other. In order for data to transfer from one asynchronous clock domain to another, there needs to be a synchronizer to capture the data reliably.

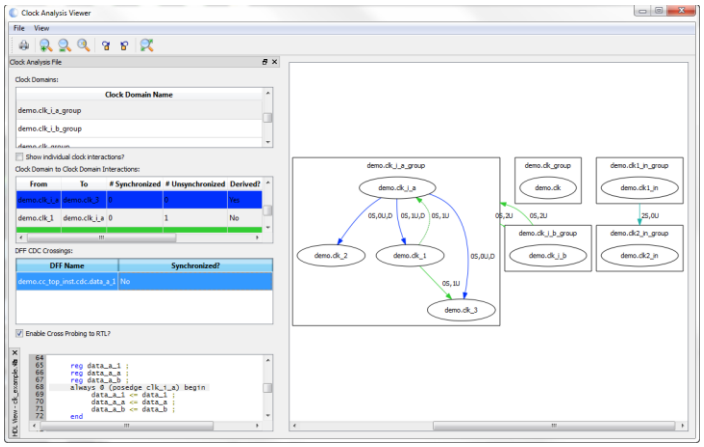


With Blue Pearl's CDC option, designers have access to

- Analyzing CDCs from a GUI or in batch mode
- Easily run CDC analysis using different scenarios
- Easy setup with specific group checks
- Full TCL parser to read in familiar inputs where clocks and domains have already been defined
- Identify synchronization issues between interacting clocks

Ease of Setup

- Blue Pearl helps ease the setup
- Automatic Clock and reset identification
- SDC input of Domain information
- Understands FPGA clock generator blocks to propagate clocks
- Advanced clock analysis diagram



CDC Analysis Types

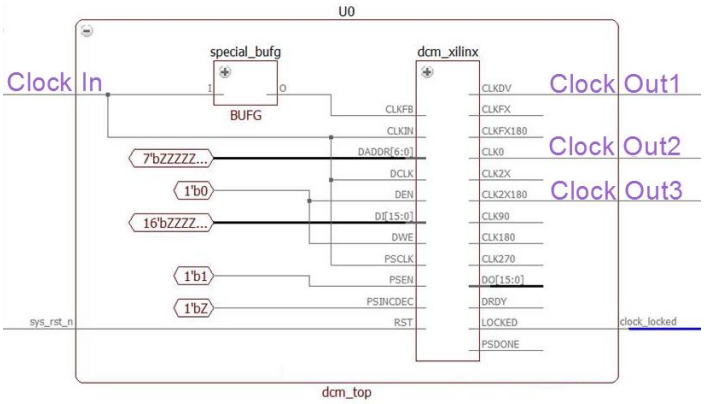
- Missing synchronizers
- Re-converging nets
- Combinational logic in synchronizers
- Combinational logic before synchronizers

Understand FPGA vendor clock schemes

Most CDC tools do not understand FPGA vendor clocking schemes. Designers thus spend enormous resources to set up their design. Blue Pearl's CDC has built-in intelligence such that with minimal effort, designers can

- Set up their CDC run
- Debug using the built-in cross-probing and schematic display.

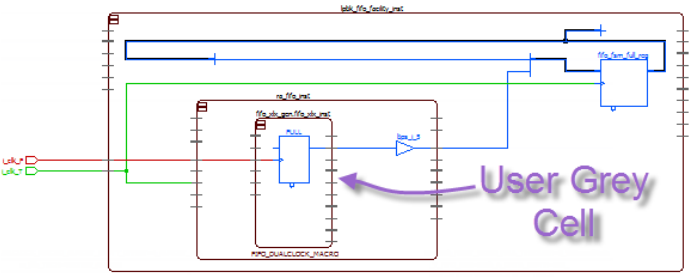
Generated clocks from FPGA IP clock distribution module are in the same domain. This eases setup and minimizes false CDCs.



Ease CDC for IP-based designs

In a typical flow, designers have to black box their generated or non-synthesizable IPs. The resulting CDC analysis is incomplete and does not report many CDC issues that lead to metastability in the field. With Blue Pearl's User Grey Cell™ (UGC) methodology, CDC issues across boundary interfaces can be identified.

- Blue Pearl release contains FPGA vendor UGC models
- UGC easy to create from databook



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