IP and FPGA Verification

Blue Pearl Software

SDC Option

Overview

The Blue Pearl Software Suite is the next generation EDA solution for IP and FPGA verification that automates RTL analysis, CDC checking, and SDC creation and validation.

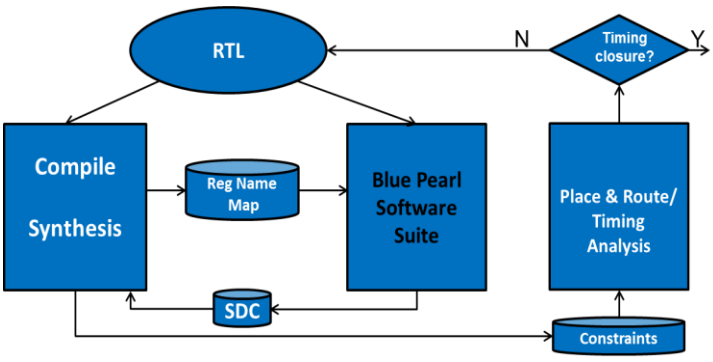
The Blue Pearl Software Suite augments existing EDA and FPGA vendor tool flows with a native Windows or Linux user experience. SDC is an option to Analyze RTL™, the base product within the software suite.

Why SDC

FPGAs routinely have millions of gates with memories, transceivers, third party IP and processor cores. They are too complex to debug in the lab. As a result, designers need verification tools that run before simulation, before synthesis, and definitely before burning chips in the lab.

ASICs and & FPGAs have many false paths and multi-cycle paths that implementation tools attempt to optimize to make timing goals. These paths can cause the critical paths to miss timing, and waste run time and system memory. Adding false path constraints frees up the synthesis tool to work only on necessary paths that will give better results for a design

Blue Pearl offers a way to automate false path generation that can be run after design changes.



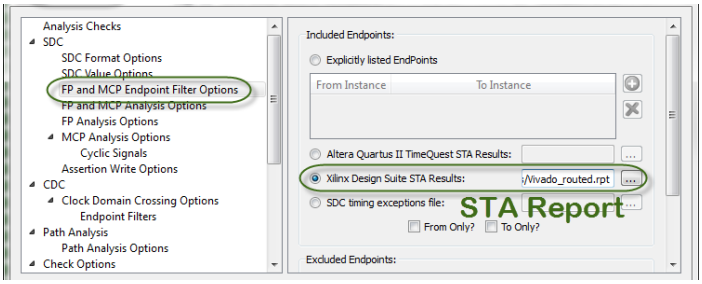
Efficient Timing Exceptions Generation

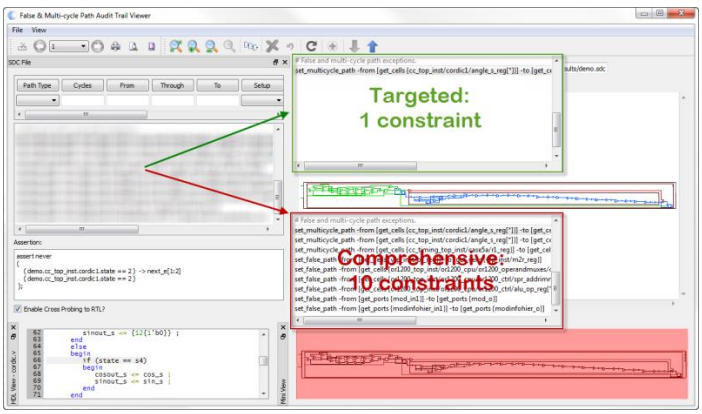
In a typical design, there may be a significant number of false paths or multi cycle paths. Passing all of them to synthesis or place & route can be very expensive and taxing to these tools. Blue Pearl's smart SDC generation

- Limits the number of exceptions generated
- Reads in critical paths information
- Accepts multiple formats

Targeted False Path and Multi Cycle Paths Constraints

There are many more false paths in a design than implementation tools can effectively use. When input as timing exception constraints, implementation tools will often use excessive memory, runtime or ignore constraints beyond some number. Blue Pearl has the ability to input critical path timing reports from Vivado and Quartus identifying select areas of the design generating false paths.

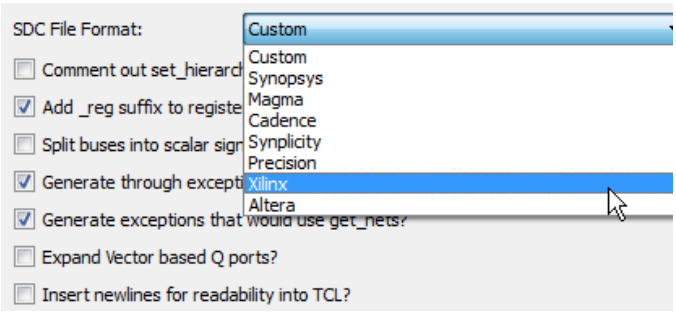




Tool Specific SDC Generated

Even though SDC is a standard format, every tool reads in a slightly different variant. However, this can limit what the tools actually process. Blue Pearl's SDC

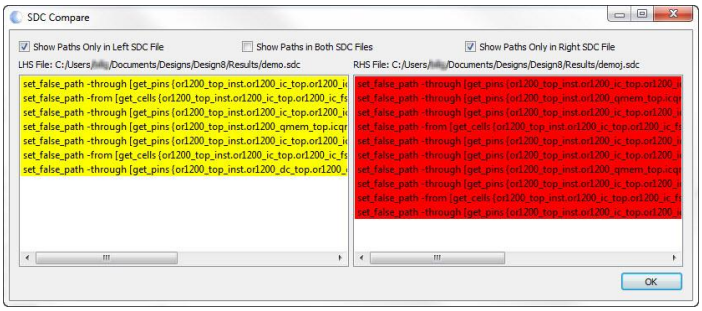
- Generates tool-specific SDC variants
- Understands the synthesis name translation
- Easily plugs into existing flow



Intelligent SDC Compare

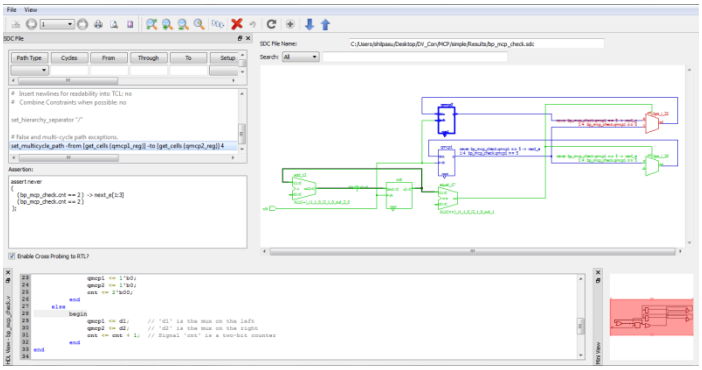
Designers perform several iterations before they close timing. It is thus important to have a mechanism to quickly compare results between runs. Blue Pearl's SDC Compare is

- Easy to use
- Provides an intelligent mechanism to track changes
- Integrated with the Visual Verification Environment™



Multi-cycle Path Generation

Multi-cycle paths are important timing constraints to be specified for a design. If not included it may be difficult or impossible for these paths to make timing. Blue Pearl has the ability to find multi-cycle paths in the design and generate an SDC constraint. Blue Pearl will also show the RTL code where the multi-cycle path is in the design and a schematic representation to help visualize the path.



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