Generate it. Prove it.
Sign off with Confidence.

AI-assisted high-reliability FPGA design and verification

Blue Pearl AI Solutions

Requirements to Bitstream

INTEGRATED VERIFICATION WORKFLOW

01 **REQUIREMENTS**

Structured specification – JIRA - DOORS

02 **GENERATE**

LLM-assisted RTL Authoring

03 **REQUIREMENTS MATCH**

Semantic implementation check

04 **STRUCTURAL ANALYSIS**

Lint, CDC, RDC, SDC, FSM

05 **FUNCTIONAL SIMULATION**

SystemVerilog, Verilog, and VHDL

06 **AUDIT EVIDENCE**

Waivers, traceability, sign-off

07 **BITSTREAM**

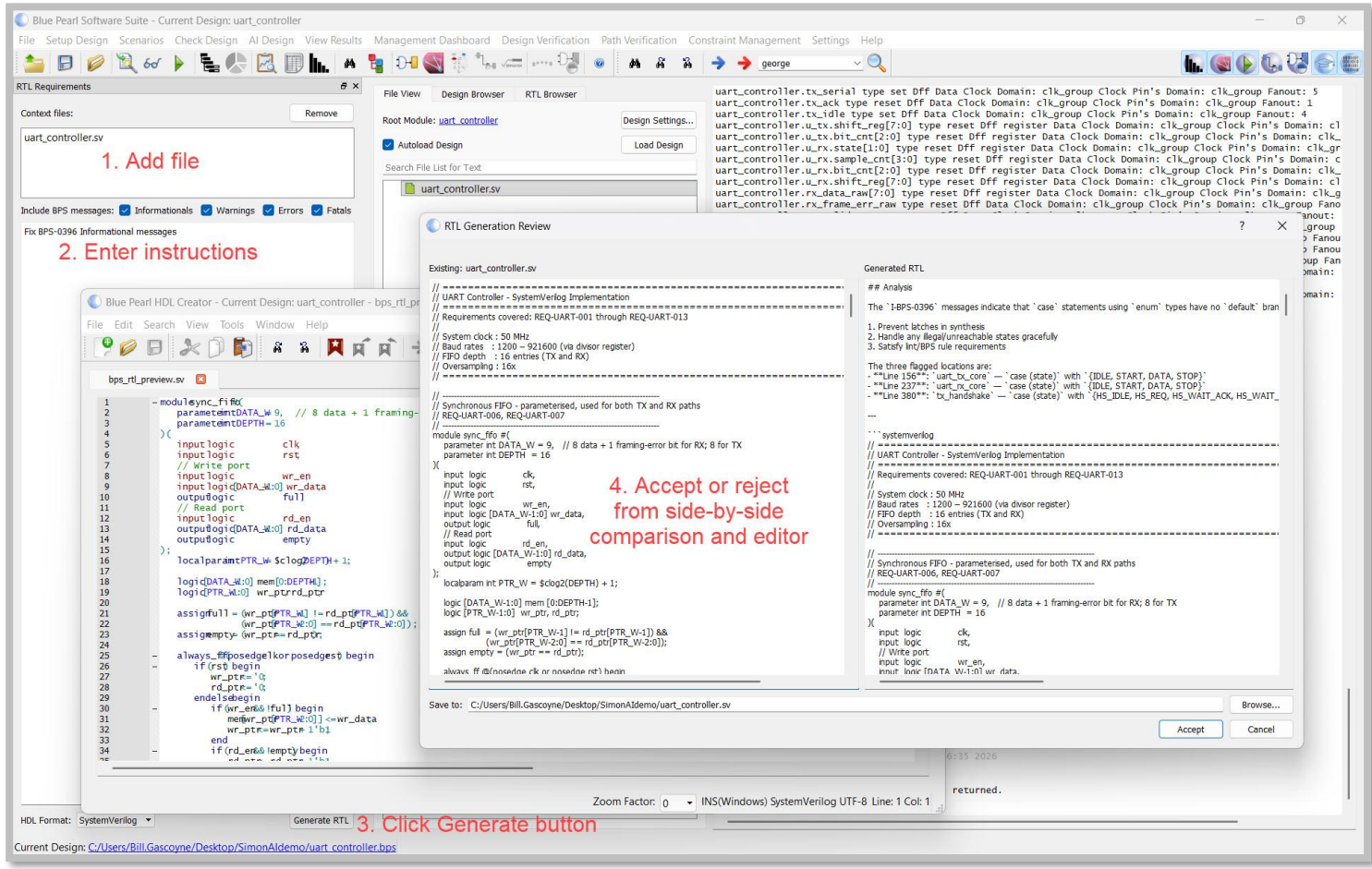
Vivado - Libero - Quartus

Blue Pearl AI Solutions

Editor and Generative AI

Natural language RTL generation

- RTL and testbench creation with generative AI
  - Smart-editor to verify as you code
  - RTL Analysis, dependency and lines of code views
  - Blue Pearl FPGA optimized LLM for on premise
  - Optional choice of your generative AI LLM
  - VSCode interface available

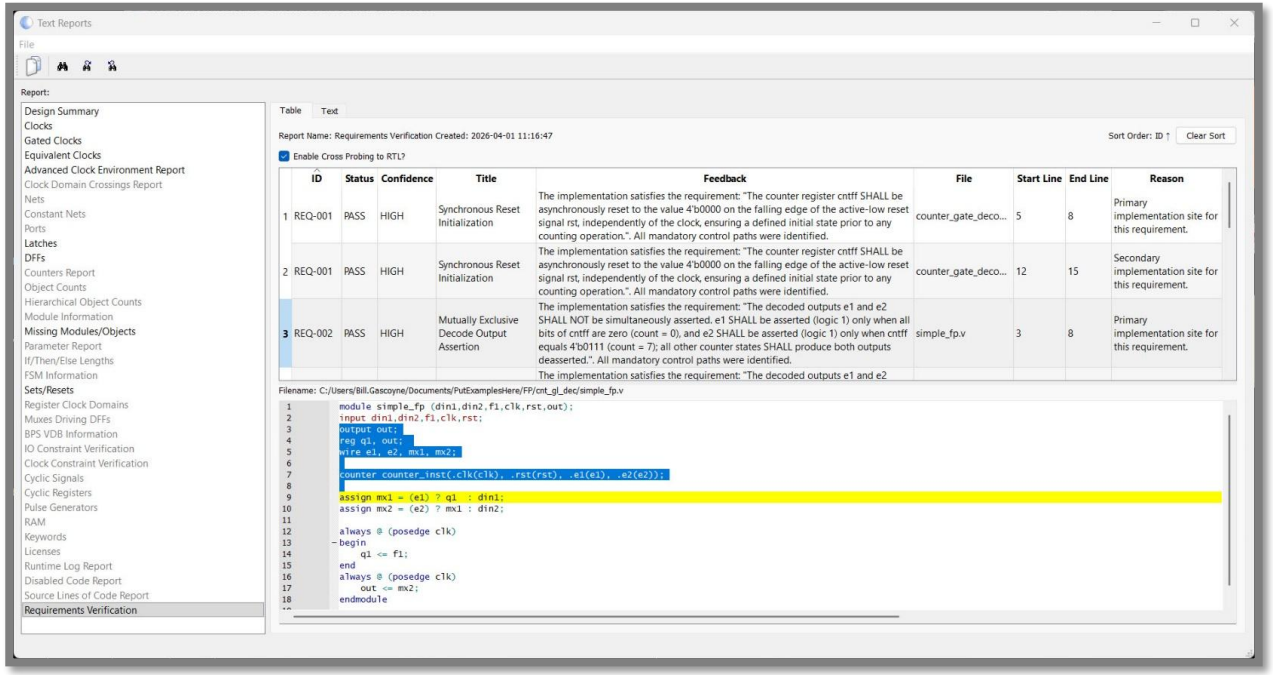


Blue Pearl AI Solutions

BPS-AI Requirements Analysis

Ensure your design meets the requirements

- Starts with the specification requirements from Doors, Jama, Enterprise Architect etc.
- Catches functional issues early in the verification cycle
  - 480 billion parameter “thinking” LLM model
  - Analyzes code against requirement to determine probability RTL implements the requirement correctly
  - Cross probes to code, to reinforce learning
- Helps with third party assessor for safety critical applications e.g. ESA / DO-254
- Future security extension to conform to EU-CRA
- Available on prem or off



Blue Pearl AI Solutions

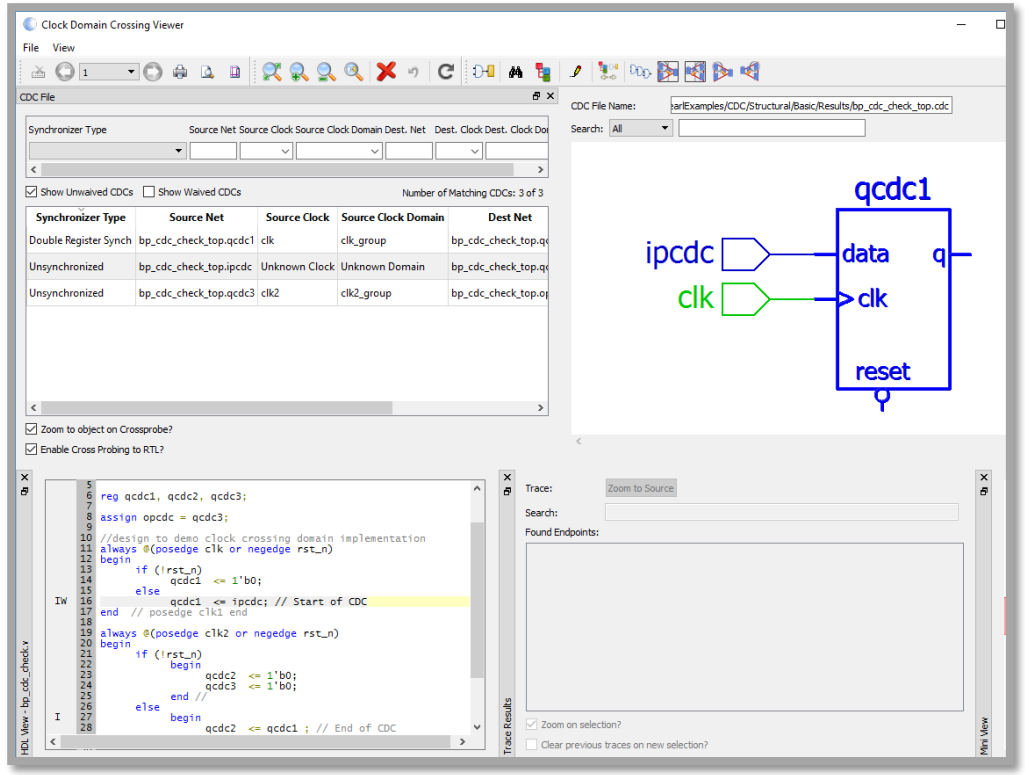
Analyze RTL AI

Clean and readable code while avoiding potential issues

- Stimulus-free advanced RTL analysis
- Integrated AI generated code fixes with your LLM of choice
- Company Specific and Industry Standard coding style checks before simulation and synthesis
- Over 400 checks that can be grouped into company-specific checklists
- Deterministic
- Includes DO-254, STARC, FPGA and ASIC packages

Clock and Reset Domain Crossing Analysis AI

Avoid metastability issues



Clock Domain Crossing Analysis

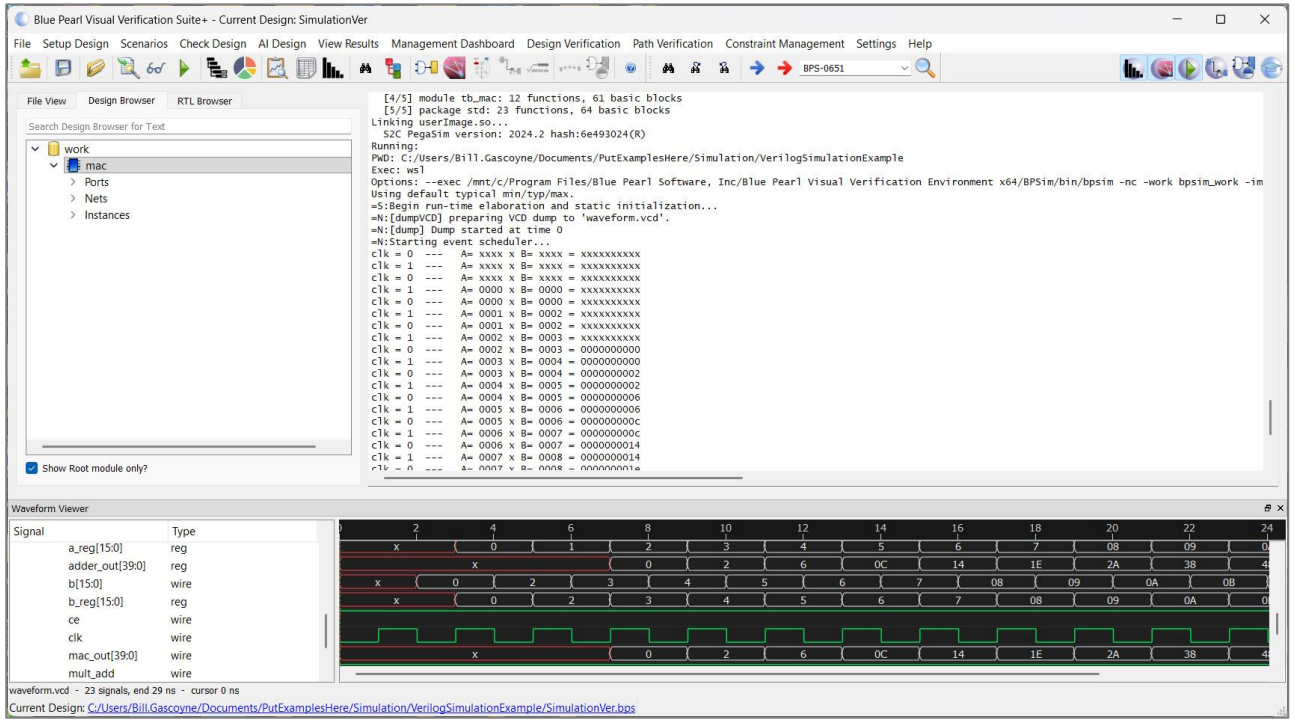
- Easily runs CDC / RDC analysis using different modes
- Integrated AI generated code fixes with your LLM of choice
- Tcl parser to read in familiar inputs where clocks and domains have already been defined
- Identifies synchronization issues between interacting clocks and reset
- Patented User Grey Cells enable verification with black boxes, encrypted and hard IP
- Generates SDC and assertions for simulation

Blue Pearl AI Solutions

BPSim – RTL Simulation

High-performance RTL simulator at a fraction of the cost

- SystemVerilog, Verilog, and VHDL
- UVM, VMM, and OVM
- Cocotb support
- SDF and timing checks
- Full DPI and VPI support
- Incremental and parallel compilation
- Competitive compilation and runtime



Blue Pearl AI Solutions

Signoff With Confidence

- An LLM can generate RTL in seconds, however it cannot produce the required certification evidence including **traceability**, **validation** and **verification**!
- Our solution is built around three tenets required for DO-254 or IEC 61508 audits

Deterministic

The same RTL, the same constraints, the same report — every run, every engineer, every machine

No probabilistic output

No drift between sessions

Auditable

Every finding traceable to a named rule

Every waiver documented with rationale

Built for the audit trail your certification authority will read

Reproducible

Identical input yields identical output, on Windows or Linux, for node-locked or floating licenses, in command line or GUI

What you sign off is what your successor will see five years from now

To schedule a private demo while at DAC, please contact info@bluepearlsolutions.com