ASIC, FPGA and IP Verification

Blue Pearl Software

SDC Generation

Overview

The Blue Pearl Software Visual Verification Suite provides enhanced Lint, Debug, Clock Domain Crossing (CDC) and automated SDC generation flows to accelerate ASIC, FPGA and IP RTL Verification on your choice of Linux or Windows.

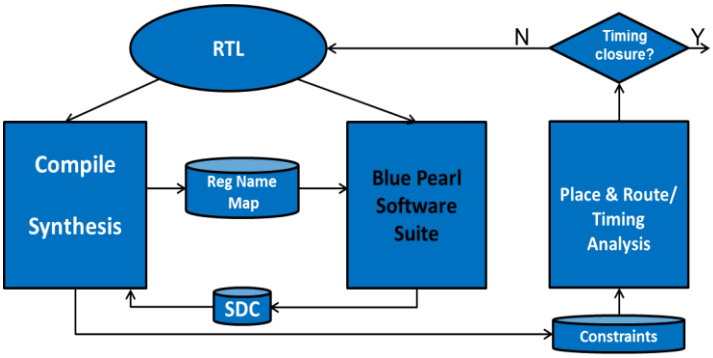
Having smarter constrains can produce higher quality designs after synthesis and place and route, while also accelerating both. The Visual Verification Suite helps find CDC, False and Multicycle paths and provides the constraints needed by synthesis to ensure the correct intended behavior augmenting existing EDA and FPGA vendor tools.

Why SDC

Today's designs routinely have millions of gates with memories, transceivers, third party IP and processor cores. They are too complex to debug in the lab. As a result, designers need verification tools that run before simulation, before synthesis, and definitely before programming chips in the lab.

ASICs and FPGAs have many false paths and multi-cycle paths that implementation tools attempt to optimize to meet timing goals. These paths can cause the critical paths to miss timing and waste run time and system memory. Adding false path constraints frees up the synthesis tool to work only on necessary paths that will give better results for a design.

Blue Pearl offers a way to automate false path generation that can be run after design changes.



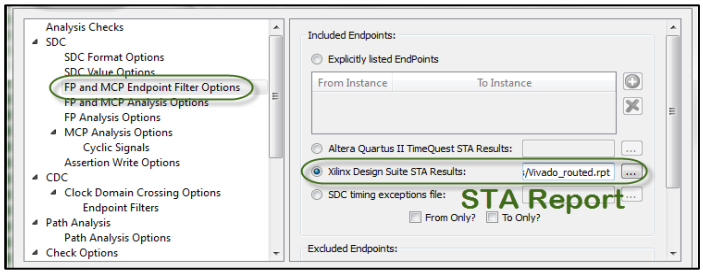
Efficient timing exception generation

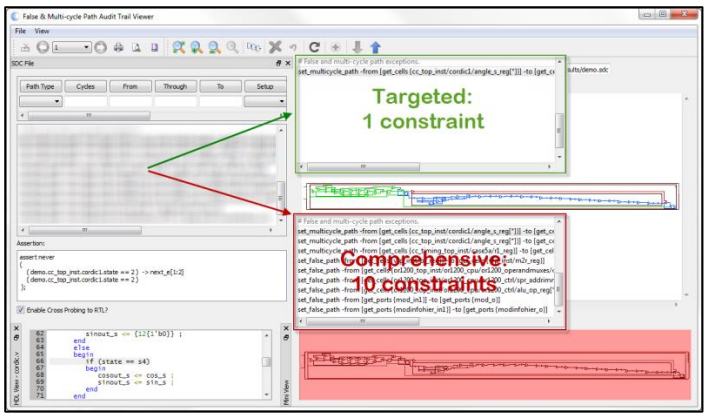
In a typical design, there may be a significant number of false paths or multi cycle paths. Passing all of them to synthesis or place & route can be very expensive and taxing to these tools. Blue Pearl's efficient SDC generation:

- Limits the number of exceptions generated
- Reads in critical path information
- Accepts multiple formats

Targeted False Path and Multi Cycle Path constraints

There are many more false paths in a design than implementation tools can effectively use. When input as timing exception constraints, implementation tools will often use excessive memory, runtime or ignore constraints beyond some number. Blue Pearl has the ability to accept critical path timing reports from Xilinx® Vivado® Design Suite and Altera® Quartus® to identify select areas of the design and generate only the most critical false path constraints.

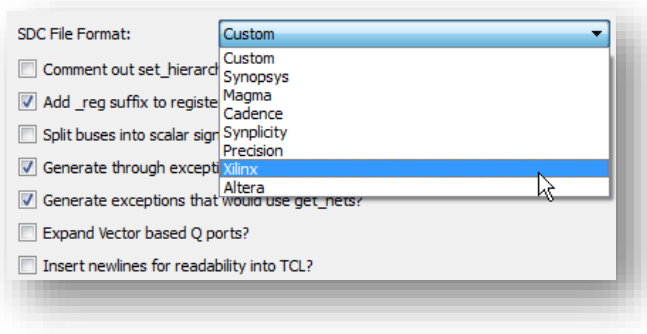




Tool specific SDC generated

Even though SDC is a standard format, every tool reads in a slightly different variant. This can limit what the tools actually process. Blue Pearl's SDC

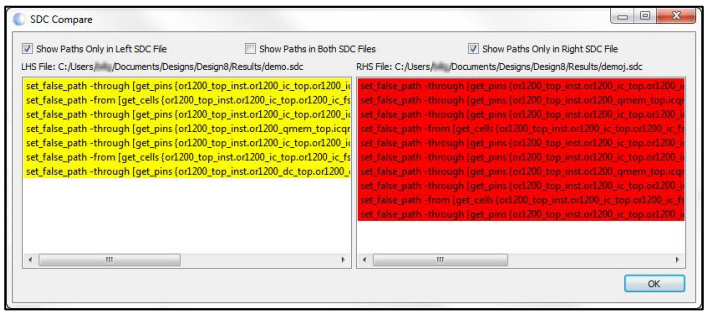
- Generates tool-specific SDC variants
- Understands the synthesis name translation
- Easily plugs into existing flows



Intelligent SDC compare

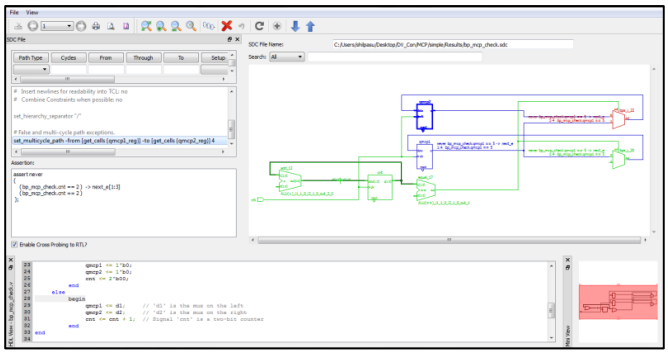
Designers perform several iterations before they close timing. It is thus important to have a mechanism to quickly compare results between runs. Blue Pearl's SDC Compare is:

- Easy to use
- Provides an intelligent mechanism to track changes
- Is integrated with the Visual Verification Suite



Multi-cycle Path generation

Muti-cycle paths (MCPs) are important timing constraints to be specified for a design. If not included it may be difficult or impossible for these paths to meet timing. Blue Pearl has the ability to find MCPs in the design and generate SDC constraints. Blue Pearl will also indicate where within the RTL code the MCP is in the design and a schematic representation to help visualize the path.



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