Blue Pearl Solutions™
ASIC, FPGA, and IP Verification

BPS 100P

Overview

Blue Pearl Solutions' BPS 100 delivers an efficient and high-performance solution for early firmware/software development and system validation. The BPS 100 features AMD Versal™ Premium VP1902 adaptive SoC with 100M ASIC gate capacity, delivers 2x logic resources and 2.5x the I/O bandwidth when compared with BPS 19P. Designed to address the growing demands of AI and HPC, the BPS-100 easily supports medium-scale to hyperscale design with exceptional performance and connectivity, making it a versatile choice for advanced chip development.

Highlights

- 100M ASIC Gate Capacity per FPGA
- Rich Memory Resources
- High-Speed & Flexible I/O Architecture with PCIe Gen5
- High Productivity Toolchain

Features

Large Capacity and Scalability

- 18,507M System Logic Cells and 858Mb of internal memory
- 6,864 DPS Slices
- Multiple Logic Systems can be conveniently connected to expand capacity

High Performance

GTM transceivers operate up to 56Gbps
GTYP transceivers operate up to 32Gbps
Multiple DDR4 channels and support up to 72-bit/32GB
Length-matched IOs

Flexible & Powerful I/O

- 2,052 XPIOs on 38 Prodigy+ connectors
- 96 XPIOs and 64 GTYPs on 16 PGT+ connectors
- 64 XPIOs and 32 GTMs on 8 MCIO connectors
- Adjustable I/O voltages from 1.0V to 1.5V

Advanced Clock Management Standalone Mode

- 18 global clocks to be selected from external clocks or internal programmable clocks
- 6 global resets to be selected from internal or external global reset sources
- 18 feedback clock outputs per FPGA

High Reliability

- High-speed I/O connectors with screw-lock design
- Self-test program to ease diagnosis of potential connectivity issues
- Automatic shutdown upon detection of over-current, over-voltage or over-temperature

Fast Time to Deployment

- Wide selection of ready-to-use daughter cards
- Proven speed adaptor solutions
- Memory Models to bridge DDR5/LPDDR5/HBM3 DFI controller to DDR4 PHY

	BPS-100
Capacity per System	Up to 100M
System Logic Cells (K)	18,507
FPGA Internal Memory (Mb)	858
DSP Slices	6,864
XPIOs	2,212
GTYP Channels	64
GTM Channels	32
Clocks	18 global clocks, 6 global resources, and 18 feedback clocks
FPGA Configuration via	JTAG, USB2.0., Ethernet, SD Card
Embedded Processor	Dual-core ARM Cortex A72, Dual-core ARM Cortex R5F
Processor I/O	Ethernet x1, SD x1, QSPI x1, UART x1, I2Cx2, PMODx1

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