



BPSim

Overview

Blue Pearl Solutions' Visual Verification Suite's BPSim is a high-performance and mixed-language digital logic simulator. BPSim utilizes innovative algorithms to achieve a high-performance simulation and constrained random solver. It supports design and verification languages including SystemVerilog, Verilog, VHDL, and UVM methodology.

Highlights

- Supports SystemVerilog, Verilog, and VHDL
- Supports UVM, VMM, and OVM methodologies
- Supports SDF and Timing Check
- Full DPI and VPI support
- Supports incremental and parallel compilation
- Competitive compilation and runtime performance



Features

- **Comprehensive language support**
 - Verilog (IEEE 1364)
 - SystemVerilog (IEEE 1800-2017)
 - Includes SVA assertions, constrained random solver, and functional coverage
 - Full DPI and VPI
 - Supports UVM methodology (IEEE 1800.2)
 - Supports UVM, VMM and OVM methodologies
 - VHDL (IEEE 1076-1993)
 - Supports std_logic_1164, numeric_std, etc.
 - Supports IP encryption (IEEE 1735)
- **Cross-language (VHDL/SV) interoperability**
 - Can instantiate VHDL inside SV, or SV inside VHDL to arbitrary depth
 - Instances can override parameters/generics
 - Appropriate type conversions on port connections
- **Code coverage**
 - Supports line/block, toggle, expression coverage analysis
 - Supports assertion coverage analysis SVA assertions
- **Multiple simulation techniques**
 - Incremental and parallel compilation
 - SDF and Timing Check Co-simulation with emulation and FPGA prototyping
- **High-performance & Mixed language**
 - VHDL, Verilog & SystemVerilog mixed simulation
 - Large-scale design simulation, such as hundreds of millions of gates
 - Competitive compilation and runtime performance

Easy to deploy and use

- Supports multiple processor architectures – X86, RISC-V, ARM
- Supports cloud deployment and parallel execution of regression tasks on the cloud
- Supports VCD and self-developed waveform formats for waveform analysis and source code debugging

Coverage Analysis

During chip validation, verification completeness is measured with RTL code coverage. BPSim integrates the coverage analysis tool to support coverage-driven verification, coverage goal reports, and coverage hole detection.

The screenshot displays a software interface for coverage analysis. On the left, a table titled "Coverage Summary" lists various RTL modules with their respective coverage metrics. The table has columns for "Name", "Line", and "Toggle". The "Line" column contains two values for each module, likely representing different coverage metrics. The "Toggle" column contains a red bar, indicating that the coverage is not 100%. A callout box labeled "Source Code & Coverage Info" points to a specific line of code in the right-hand pane, which shows a snippet of Verilog code. The code includes several conditional statements and assignments, with line numbers 793 through 818 visible. The code is color-coded, with some lines highlighted in red and others in yellow. The interface also shows a menu bar with "File", "View", and "Help" options, and a toolbar with icons for file operations and search.

Name	Line	Toggle
ct_biu_snoop_channel	87.05	7.10
ct_biu_top		92.79
ct_biu_write_channel	78.31	24.10
ct_ciu_apbif	80.47	5.08
ct_ciu_bmbif		38.28
ct_ciu_bmbif_kid	100.00	30.95
ct_ciu_ctcq	88.44	3.33
ct_ciu_ctcq_reqq_entry	73.28	1.61
ct_ciu_ctcq_respq_entry	89.74	6.58
ct_ciu_ebiuif	100.00	46.23
ct_ciu_l2cif	74.71	72.47
ct_ciu_ncq	85.77	17.19
ct_ciu_ncq_gm	76.92	15.47
ct_ciu_regs	84.00	4.87
ct_ciu_regs_kid	89.23	3.54
ct_ciu_cnh		81.68

```
793 1 ncq_ar_apbif_sel <= 1'b0;
794 1 else if (apbif_ncq_ar_grant)
795 0 ncq_ar_apbif_sel <= 1'b1;
796 1 else if (ncq_apbif_r_grant)
797 0 ncq_ar_apbif_sel <= 1'b0;
805 1 if (!cpurst_b)
806 1 ncq_ar_ebiu_so_sel <= 1'b0;
807 1 else if (ebiu_ncq_ar_so_grant && !ncq_ebiu_r_so_grant)
808 0 ncq_ar_ebiu_so_sel <= 1'b1;
809 1 else if (!ebiu_ncq_ar_so_grant && ncq_ebiu_r_so_grant)
810 0 ncq_ar_ebiu_so_sel <= 1'b0;
815 1 if (!cpurst_b)
816 1 ncq_ar_ebiu_ostd_cnt[4:0] <= 5'b0;
817 1 else if (ebiu_ncq_ar_grant && !ncq_ebiu_r_grant)
818 0 ncq_ar_ebiu_ostd_cnt[4:0] <= ncq_ar_ebiu_ostd_cnt[4:0] + 5'b1;
```

Request a [Demo](#) today!

Contact us:

www.bluepearlsoftware.com

+1(408) 961 0121

sales@bluepearlsoftware.com