Blue Pearl Solutions™
ASIC, FPGA, and IP Verification

BPSim

Overview

Blue Pearl Solutions' Visual Verification Suite's BPSim is a high-performance and mixed-language digital logic simulator. BPSim utilizes innovative algorithms to achieve a high-performance simulation and constrained random solver. It supports design and verification languages including SystemVerilog, Verilog, VHDL, and UVM methodology.

Highlights

- Supports SystemVerilog, Verilog, and VHDL
- Supports UVM, VMM, and OVM methodologies
- Supports SDF and Timing Check
- Full DPI and VPI support
- Supports incremental and parallel compilation
- Competitive compilation and runtime performance

Features

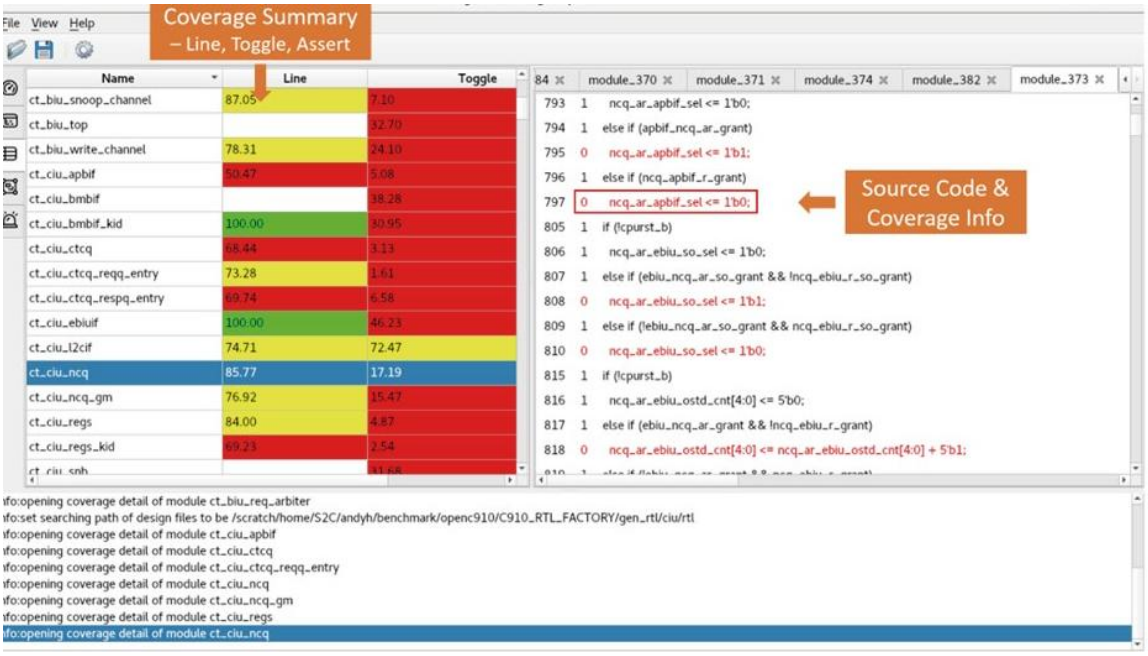
- **Comprehensive language support**
  - Verilog (IEEE 1364)
  - SystemVerilog (IEEE 1800-2017)
    - Includes SVA assertions, constrained random solver, and functional coverage
    - Full DPI and VPI
  - Supports UVM methodology (IEEE 1800.2)
    - Supports UVM, VMM and OVM methodologies
  - VHDL (IEEE 1076-1993)
    - Supports std_logic_1164, numeric_std, etc.
    - Supports IP encryption (IEEE 1735)
- **Cross-language (VHDL/SV) interoperability**
  - Can instantiate VHDL inside SV, or SV inside VHDL to arbitrary depth
  - Instances can override parameters/generics
  - Appropriate type conversions on port connections
- **Code coverage**
  - Supports line/block, toggle, expression coverage analysis
  - Supports assertion coverage analysis SVA assertions
- **Multiple simulation techniques**
  - Incremental and parallel compilation
  - SDF and Timing Check Co-simulation with emulation and FPGA prototyping
- **High-performance & Mixed language**
  - VHDL, Verilog & SystemVerilog mixed simulation
  - Large-scale design simulation, such as hundreds of millions of gates
  - Competitive compilation and runtime performance

Easy to deploy and use

- Supports multiple processor architectures – X86, RISC-V, ARM
- Supports cloud deployment and parallel execution of regression tasks on the cloud
- Supports VCD and self-developed waveform formats for waveform analysis and source code debugging

Coverage Analysis

During chip validation, verification completeness is measured with RTL code coverage. BPSim integrates the coverage analysis tool to support coverage-driven verification, coverage goal reports, and coverage hole detection.



Request a Demo today!

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